DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

1. Claims 1-5, 22 are rejected under 35 U.S.C. 103(a) as being anticipated by US 5717226 to Lee et al., in view of Huang et al., USPAT 6,693,352.

Regarding claim 1, Lee discloses a light-emitting diode chip in fig. 3C having an epitaxial semiconductor layer sequence (31/32/33/34) with an active zone 32, column 3 line 27, that emits electromagnetic radiation and an electrical contact structure comprising a radiation-transmissive electrical current expansion layer 35 comprising ZnO, column 3 line 31, and having a front side surface which faces away from the semiconductor layer sequence; and an electrical connection layer 36, column 4 line 5, wherein the current expansion layer 35 is applied directly on a cladding layer 34 of the semiconductor layer and comprises a window, in which the connection layer 36 is applied on said cladding layer 34, and said cladding layer is p-doped, col. 3 line 28; wherein the connection layer 36 is electrically conductively connected to the current expansion layer 35, and does not cover or only partly covers the front side surface of the current expansion layer 35, and wherein junction between the connection layer 36 and the cladding layer 33, during the operation of the light-emitting diode chip, is not electrically conductive, column 3 line 3 line 60-65, or is only poorly electrically conductive such that an entire, or virtually the entire, current from the connection layer 36 flows via the current expansion layer 35 into the semiconductor layer sequence.

Lee differs from the claimed invention because he does not explicitly disclose an LED device having a cladding layer that is the only layer of the semiconductor layer sequence that is adjacent to said connection layer within said window.

Huang shows in fig.7, an LED device having a P-layer (35)(col.4,line 49) that is the only layer of the semiconductor layer sequence that is adjacent to said connection layer (37a)(col.4,line 51) within said window.

Huang is evidence that ordinary skilled in the art would find reasons, suggestions or motivation to modify the device of Lee. Therefore, it would have been obvious at the time the invention was made to have an LED device having a cladding layer that is the only layer of the semiconductor layer sequence that is adjacent to said connection layer within said window teaching of Huang in it's device because it would provide a device with low resistance because of the direct contact to the semiconductor layer, as taught by Huang (col.2,line 46-50).

> Although the prior art does not specially disclose the during the operation of the light-emitting diode chip, is not electrically conductive or is only poorly electrically conductive such that an entire, or virtually the entire, current from the connection layer flows via the current expansion layer into the semiconductor layer sequence limitation, this feature is seen to be inherently teaching of that limitation because Lee discloses the material and structure substantially identical to claimed invention, claimed properties or functions are presumed to be inherent. *In re Best*, 195 USPQ 430, 433 (CCPA 1977).

Regarding claim 2, Lee discloses the light-emitting diode chip according to claim 1, wherein the connection layer 36 comprises a metal, column 4 line 5, and the junction between the connection layer 36 and the cladding layer 33 comprises an electrical potential barrier, column 3 line 60-65.

Regarding claims 3-4, 22 Lee discloses the light-emitting diode chip according to claim 1, the sheet resistance of intermediate layers of the semiconductor layer sequence between the active zone and the electrical contact structure is greater than or equal to 200 Ω /sq, wherein the current expansion layer 35 comprises a sheet resistance of less than or equal to 190 Ω /sq or 30 Ω/sp.

Although the prior art does not specially disclose the sheet resistance limitation, this feature is seen to be inherently teaching of that limitation because Lee discloses the material and structure substantially identical to claimed invention, claimed properties or functions are presumed to be inherent. *In re Best*, 195 USPQ 430, 433 (CCPA 1977).

Regarding claim 5, Lee discloses the light-emitting diode chip according to claim 1, wherein the connection layer 36 extends beyond the window on a side of the current expansion layer 35 which is remote from the semiconductor layer sequence (31/32/33) and is applied to a front-side surface of the current expansion layer 35 so as to partly cover the current expansion layer 35 and so that the junction between the connection layer 36 and the current expansion layer 35 is electrically conductive in this region, fig. 3C.

Regarding claims 6, Lee discloses the light-emitting diode chip wherein the semiconductor layer sequence is based on AlGaInP, column 25-28.

But Lee does not discloses the semiconductor layer $In_xGa_yAl_{1-x-y}P$ where $0 \leq x \leq 1$, $0 \leq y \leq 1$ and $x + y \leq$

However, Huang discloses the semiconductor layer $Al_xGa_yIn_{1-x-y}P_{1-z}$ where $0 \leq x \leq 1$, $0 \leq y \leq 1$, $0 \leq x + y \leq 1$, and $0 \leq z \leq 1$. Accordingly, it would have been obvious to one of ordinary skill in art to use the semiconductor layer teaching of Huang in Lee's device in the range as claimed, because it has been held that where the general conditions of the claims are discloses in the prior art, it is not inventive to discover the optimum or workable range by routine experimentation. See In re Aller, 220 F.2d 454, 105 USPQ 233, 235 (CCPA 1955); *Merck & Co. Inc. v. Biocraft Laboratories Inc.*, 874 F.2d 804, 10 USPQ2d 1843 (Fed. Cir.), *cert. denied*, 493 U.S. 975 (1989); *In re Kulling*, 897 F.2d 1147, 14 USPQ2d 1056 (Fed. Cir. 1990); *In re Geisler,* 116 F.3d 1465, 43 USPQ2d 1362 (Fed. Cir. 1997); *In re Boesch*, 617 F.2d 272, 205 USPQ 215 (CCPA 1980); MPEP 2144.05.

2. Claims 7-9, 23-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 5717226 to Lee and Huang as applied to claims 1-6, 22 and further in view of et al. to US Pub 2003/0059972 to Ikeda et al. of record.

Regarding claims 7, 23, Lee discloses the light-emitting diode chip according to claim 1, wherein the cladding layer 34 comprises AlGaAs, column 4 line 28.

But Lee does not disclose the cladding layer comprises $Al_xGa_{1-x}As_yP_{1-y}$ where $0 \leq x \leq 1$ and $0 \leq y \leq 1$ and where $0.1 \leq x \leq 0.5$ and $y = 1$ or where $x=0$ and $y=0$.

However, Ikeda discloses the cladding layer can comprise AlGaAs, GaInP, and AlGaInP [0033]. At the time of the invention was made; it would have

been obvious to one of ordinary skill in the art to combine the cladding layer teaching of Ikeda to replace the cladding layer of Lee, because such material substitution would have been considered a mere substitution of art-recognized equivalent values, MPEP 2144.06. With respect to the x any y concentration, it would have been obvious to one of ordinary skill in art to combine the teaching of Lee and Ikeda in the range as claimed, because it has been held that where the general conditions of the claims are discloses in the prior art, it is not inventive to discover the optimum or workable range by routine experimentation. See In re Aller, 220 F.2d 454, 105 USPQ 233, 235 (CCPA 1955); *Merck & Co. Inc. v. Biocraft Laboratories Inc.*, 874 F.2d 804, 10 USPQ2d 1843 (Fed. Cir.), *cert. denied*, 493 U.S. 975 (1989); *In re Kulling*, 897 F.2d 1147, 14 USPQ2d 1056 (Fed. Cir. 1990); *In re Geisler,* 116 F.3d 1465, 43 USPQ2d 1362 (Fed. Cir. 1997); *In re Boesch*, 617 F.2d 272, 205 USPQ 215 (CCPA 1980); MPEP 2144.05.

Regarding claim 8, Lee does not discloses the light-emitting diode chip according to claim 7 wherein the cladding layer is p-doped with at least one of a the dopant Zn and C.

However, Lee discloses layer 34 is P-type cladding layer. At the time the invention was made; it would have been obvious to one of ordinary skill in the art to understand that Zn would be a typical material used in the art as a dopant of p-type for cladding layer, see Wang (6469324) column 2 lines 26, Sasaki (6074889) column 1 lines 48-51, or Takeoka (5789773) column 1 line 61.

Regarding claims 9, 24 Lee doe not disclose the light-emitting diode chip wherein the layer cladding layer is doped with a dopant concentration of between about $1x10^{18}$.

However, Lee discloses the doping concentration of a material is about $1x10^{18}$ cm^{-3}, column 1 line 44. Accordingly, it would have been obvious to one of ordinary skill in art to use doping teaching of Lee in the range as claimed, because it has been held that where the general conditions of the claims are discloses in the prior art, it is not inventive to discover the optimum or workable range by routine experimentation. See In re Aller, 220 F.2d 454, 105 USPQ 233, 235 (CCPA 1955); *Merck & Co. Inc. v. Biocraft Laboratories Inc.*, 874 F.2d 804, 10 USPQ2d 1843 (Fed. Cir.), *cert. denied*, 493 U.S. 975 (1989); *In re Kulling*, 897 F.2d 1147, 14 USPQ2d 1056 (Fed. Cir. 1990); *In re Geisler*, 116 F.3d 1465, 43 USPQ2d 1362 (Fed. Cir. 1997); *In re Boesch*, 617 F.2d 272, 205 USPQ 215 (CCPA 1980); MPEP 2144.05.

3. Claims 10-13, 25-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 5717226 to Lee and Huang as applied to claims 1-6, 22 and further in view of Udagawa et al. of record.

Regarding to claims 10-13, 25-26 Lee discloses the current expansion layer 35 has general thickness.

But Lee does not discloses the current expansion layer comprises Al, wherein the proportion of Al between 0% and 10%, wherein the thickness between 100-600 nm or the thickness corresponding about a quarter of the wavelength of a radiation emitted by the light-emitting diode chip.

However, Udagawa discloses the light-emitting diode in fig. 6 wherein the expansion layer 406 comprises Al, column 8 line 56, wherein the proportion of Al between 1% and 10%, column 8 line 57, wherein the thickness between 100-600 nm, column 8 line 64. At the time the invention was made; it would have been obvious to one of ordinary skill in the art to use the ZnO:Al layer 406 teaching of Udagawa with Lee's device, because Al doped ZnO would have created a specific resistance level for layer ZnO as taught by Udagawa, column 8 line 59.

4. Claims 14-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 5717226 to Lee and Huang as applied to claims 1-6, 22 and further in view of et al. to JP 2001036131 to Udagawa of record.

Regarding claims 14-21, Lee does not discloses the light emitting diode wherein the current expansion layer is provided with watertight material such that the current expansion layer is adequately protected against moisture, wherein watertight material is applied to free areas of the contact layer, wherein watertight material is applied to all the free areas of the contact layer, wherein the watertight material is a dielectric that is transparent to an electromagnetic radiation emitted by the light-emitting diode chip, wherein the dielectric comprises one or more of the substances Si_xN_y, SiO, SiO_2, Al_2O_3 and SiO_xN_y, 19, wherein a refractive index of the watertight material is less than the refractive index of the current expansion layer and is adapted so as to significantly minimized reflections of the radiation emitted by the light-emitting diode chip at interfaces with respect to the watertight material, wherein the current expansion layer has a thickness corresponding to about an integer multiple of half the wavelength of a

radiation emitted by the light-emitting diode chip, and the watertight material has a thickness corresponding to about a quarter of said wavelength, wherein the thickness of the watertight material is in a range of between 50 and 200 nm inclusive.

However, Udagawa discloses the light emitting diode in fig. 1 wherein the current expansion layer 107 is provided with watertight material 108 in such a way that it is adequately protected against moisture, wherein watertight material is applied to free areas of the contact layer, wherein watertight material 108 is applied to all the free areas of the contact layer, wherein the watertight material 108 is a dielectric that is transparent to an electromagnetic radiation emitted by the light-emitting diode chip, wherein the dielectric comprises one or more of the substances Si_xN_y, SiO, SiO_2, Al_2O_3 and SiO_xN_y, see abstract, wherein the refractive index of the watertight material is less than the refractive index of the current expansion layer and is adapted to the greatest possible extent in particular for a minimization of reflections of the radiation emitted by the light-emitting diode chip at interfaces with respect to the watertight material, see abstract, wherein the current expansion layer 107 has a general thickness, wherein the thickness of the watertight material 108 has a general thickness. At the time the invention was made; it would have been obvious to one of ordinary skill in the art to use the watertight layer teaching of Udagawa with Lee's device, because it would have provided the protection and improved light emitting efficiency as taught by Udagawa, see abstract.

With respect to the thickness, it would have been obvious to one of ordinary skill in art to use the general thickness teaching of Udagawa with Lee's device in the range as claimed, because it has been held that where the general conditions of the claims are discloses in the prior art, it is not inventive to discover the optimum or workable range by routine experimentation. See In re Aller, 220 F.2d 454, 105 USPQ 233, 235 (CCPA 1955); *Merck & Co. Inc. v. Biocraft Laboratories Inc.*, 874 F.2d 804, 10 USPQ2d 1843 (Fed. Cir.), *cert. denied*, 493 U.S. 975 (1989); *In re Kulling*, 897 F.2d 1147, 14 USPQ2d 1056 (Fed. Cir. 1990); *In re Geisler,* 116 F.3d 1465, 43 USPQ2d 1362 (Fed. Cir. 1997); *In re Boesch*, 617 F.2d 272, 205 USPQ 215 (CCPA 1980); MPEP 2144.05.

Response to Arguments

5. Applicant's arguments with respect to claims 1-26 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to MARC ARMAND whose telephone number is (571)272-9751. The examiner can normally be reached on Monday - Friday between 9-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on 571-272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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